

REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed September 28, 2004.

Currently, claims 1-36 are pending. Applicants have amended claims 1, 2, 10, 16, 25, 27, 32, 33, and 34. Applicants respectfully request reconsideration of claims 1-36.

I. Summary of the Examiner's Objections

Claim 2 is rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-3, 5-17, 19, 20 and 25-36 are rejected under 35 USC 102(b) as being anticipated by Morishita (6,329,873).

Claims 4 and 18 are rejected under 35 USC 103(a) as being unpatentable over Morishita (6,329,873) in view of Hellums (5,362,988).

II. Summary of the Amendments

Claims 1, 2, 10, 16, 25, 27, 32, 33, and 34 have been amended.

III. Remarks

Claim 2 has been amended. It is respectfully submitted that the rejection of claim 2 under 35 USC Section 112 is now moot in view of the amendment. Claims 27 and 33 have been amended. It is respectfully submitted that the objections to claims 27 and 33 have been rendered moot by the amendments thereto.

There is No Anticipation of the Claimed Invention By Morishita

It is respectfully submitted that the invention as defined in claims 1-3, 5-17, 19, 20 and 25-36 is not anticipated by Morishita (6,329,873).

The invention is not anticipated by Morishita since Morishita fails to disclose a "bypass" or "... a bypass enable signal operable responsive to a signal generated by the host device

indicating that the power up of the host is complete".

- The Examiner's reliance on device 1h of Morishita as a "bypass" is misplaced: this device 1h operates in parallel with the regulation circuit, and hence is not a bypass or "short".
- The Examiner's reliance on the ACT signal in Morishita is misplaced, as the ACT signal is clearly under control of the host in a manner unrelated to an indication that the power up is complete.

Each of these positions is further clarified below.

Claims 1 – 3, 5-15.

It is respectfully submitted that claims 1 – 15 are not anticipated by Morishita. Claim 1 requires

... a bypass shorting the host voltage at the input to the output;
a bypass enable signal operable *responsive to a signal generated by the host device indicating that the power up of the host is complete.* (emphasis supplied)

Morishita does not operate in response to a signal that the device has completed powering up, nor does it operate to provide a bypass as claimed.

The passage "a bypass shorting the host voltage at the input to the output" finds support in the specification at page 10, paragraphs 0035 and 0036, which indicates that:

...., the ability to short the supply voltage at the input to the output in any regulator configuration is utilized to implement the invention. (0035, lines 6 – 7)

.... Upon application of a BYPASS signal, under the direction of the controller 160, the bypass transistor shorts the input voltage between VDD and the output. Thus, in cases where the input voltage is sufficient to operate the memory system, the bypass is enabled and the voltage is provided directly to the output. In cases where the voltage is significantly higher, the voltage regulator is allowed to operate normally to reduce the voltage supplied to the output. (0036, lines 6 – 12)

There is no disclosure of such a bypass in Morishita. In particular, in Morishita, the **1h** transistor is not a bypass, shorting transistor, but when enabled, transistor **1h** operates with the

regulator DRm. This is known because Morishita discloses that **1h** operates in parallel *in parallel* with the current drive transistor **DRm**, and the size of the transistor DRM in the third embodiment plus the size of 1h is equivalent to **DRm** alone in two previous embodiments:

...auxiliary drive transistor 1h provided parallel to current drive transistor DRm and formed of a p channel MOS transistor for supplying current from external power supply node EXV to internal power supply line IVL when made conductive. The size DRm (current supply ability: gate width) of current drive transistor is set smaller than the size of current drive transistor DRM of the first and second embodiments. The current drivability (size: channel width) of MOS transistor 1h is set smaller than that of current drive transistor DRm. **The total size (channel width) of current drive transistor DRm and MOS transistor 1h for level adjustment is set equal to the size (channel width) of the current drive transistor DRM of the first and second embodiments.** Col. 15 line 69 – col.16 line13. (Emphasis supplied).

When the difference between external power supply voltage ExtVcc and reference voltage Vref becomes smaller to reduce the gain of main amplifier MA so that the difference between internal power supply voltage IntVcc and reference voltage Vref becomes greater, lower limit detection signal SIG from lower limit detection circuit 1a attains an H level. In response, lower limit detection signal ZSIG from inverter 1g attains an L level. Level adjusting MOS transistor 1h is turned on, and current is supplied from external power supply node EXV to internal power supply line IVL. Reduction in the drivability of current drive transistor DRm is compensated for by level adjusting MOS transistor 1h to suppress reduction in the voltage level of internal power supply voltage IntVcc. The size (channel width) of level adjusting MOS transistor 1h is set small and the current drivability thereof is relatively small. Therefore, it is prevented that a great current is rapidly supplied to internal power supply line IVL when level adjusting MOS transistor 1h is turned on to suddenly raise the level of internal power supply voltage IntVcc (ringing suppression). **The size (channel width) of level adjusting MOS transistor 1h is set small and the current drivability thereof is relatively small. Therefore, it is prevented that a great current is rapidly supplied to internal power supply line IVL when level adjusting MOS transistor 1h is turned on to suddenly raise the level of internal power supply voltage IntVcc (ringing suppression).** Col. 16, lines 43 - 63 (Emphasis supplied).

In addition, the ACT signal is not “...a bypass enable signal operable *responsive to a signal generated by the host device indicating that the power up of the host is complete.*” Rather, the ACT signal is controlled by the semiconductor device dependent on the operation of the device:

When the semiconductor integrated circuit device is a dynamic random access memory, activation control circuit 2 controls activation/inactivation of activation control signal ACT, according to a row address strobe signal/RAS defining a memory cycle, or a column address strobe signal/CAS designating an initiation of a column select operation. When an operation mode is specified in the form of an external command such as in a synchronous semiconductor memory device, activation control circuit 2 may render activation control signal ACT active/inactive in response to an active command designating an initiation of a memory cycle or a read/write command designating data writing/reading. Col. 9, lines 41 – 52.

In contrast, a “a signal generated by the host indicating that the power up of the host is complete” is supported in the specification by the following language:

... where the device is an MMC card, this signal may be CMD0 or CMD1, the initial two commands sent by a host to an MMC card which are generally used to reset all cards to idle state and request and confirm operating conditions. In other technologies, any initial signal indicating the completion of power up of the host device, specifically designed for that purpose or indicating completion by its nature may be used as the indicator signal. Specification, Page 10, paragraph 0041.

Hence, Morishita does not disclose either “... a bypass shorting the host voltage at the input to the output” or “...a bypass enable signal operable responsive to a signal generated by the host device indicating that the power up of the host is complete.”

It is therefore respectfully submitted the invention as defined in claim 1 is not anticipated by Morishita. It is further respectfully submitted that claims 2– 3, 5-15 being dependent from claim 1 and including all the limitations of claim 1, are likewise not anticipated for the reasons set forth above.

Claims 16, 17, 19, 20

It is respectfully submitted that claims 16 – 24 are not anticipated by Morishita. Claim 16 requires the steps of:

providing ... a regulator bypass shorting the host voltage at the input to the output responsive to an enable signal;

...
responsive to *a power up completion signal from a host device, determining the power supplied by the host;* (emphasis added)

Morishita does not provide “...a regulator bypass shorting the host voltage at the input to the output.” As noted above, neither device 1h, cited by the Examiner as teaching a bypass, nor any other element in Morishita constitutes such a device. Likewise, neither the ACT signal, nor any other signal disclosed in Morishita, constitutes a “power up completion signal”, as discussed above with respect to claim 1.

It is therefore respectfully submitted the invention as defined in claim 16 is not anticipated by Morishita. It is further submitted that the invention defined in claims 17, 19, 20,

being dependent from and including all the limitations of claim 16, is likewise not anticipated by Morishita.

Claims 25 – 31

It is further respectfully submitted that claims 25 - 31 are not anticipated by Morishita. Morishita does not disclose:

a bypass element coupled to selectively short the host voltage at the input to the output;

a bypass control signal coupled to the bypass element and responsive to a host system power up completed signal which enables the bypass element when the host voltage provided by the host is below a threshold level.

As noted above with respect to claim 1, Morishita does not disclose whether the bypass element or, in claim 25, a "...bypass control signal... responsive to a host system power up completed signal".

It is therefore respectfully submitted the invention as defined in claim 25 is not anticipated by Morishita. It is further submitted that the invention defined in claims 36 - 31 being dependent from and including all the limitations of claim 25 are likewise not anticipated by Morishita.

Claims 32 – 33

It is further respectfully submitted that claims 32 – 33 are not anticipated by Morishita. Morishita does not disclose:

providing a regulator bypass shorting the a host voltage at the input to the output;

setting the bypass to off prior to power up of a host device;
responsive to a command signal from the host device, determining the power supplied by the host; and

if the power is below a threshold operating voltage, enabling the bypass.

As noted above with respect to claim 1, Morishita does not disclose whether the bypass element or, the step of determining "responsive to a command signal". In Morishita, the

determining step is completed continuously by the “lower level detection circuit” which provides the SIG and ZSIG signal to the 1h device. This is explained in Morishita in discussing the operation of the Main amplifier with respect to the first embodiment, which is still valid in the embodiment disclosing the 1h transistor:

..., when activation control signal ACT is inactive, main amplifier MA maintains an inactive state irrespective of the logic level of lower limit detection signal SIG even when lower limit detection circuit 1a carries out a detection operation so that lower limit detection signal SIG is driven to an H level/L level according to the detection result. Col. 10, lines 45 – 55.

It is therefore respectfully submitted the invention as defined in claim 32 is not anticipated by Morishita. It is further submitted that the invention defined in claim 33 being dependent from and including all the limitations of claim 32 is likewise not anticipated by Morishita.

Claims 34 – 36

It is further respectfully submitted that claims 34 – 36 are not anticipated by Morishita. Morishita does not disclose:

a voltage regulator having a shorting element between an host voltage input and an output, the shorting element being responsive to a bypass control signal, the bypass control signal provided by the controller responsive to a host system power up complete signal which enables the bypass shorting element when the host supply voltage provided by the host is below a threshold level.

As noted above with respect to claim 1, Morishita does not disclose either the shorting element or the bypass control signal which is “responsive to a host system power up complete signal”. For the reasons set forth above with respect to claim 1, it is respectfully submitted claim 34 is not anticipated by Morishita.

It is therefore respectfully submitted the invention as defined in claim 34 is not anticipated by Morishita. It is further submitted that the invention defined in claims 35 - 36 being dependent from and including all the limitations of claim 34 are likewise not anticipated by Morishita.

Neither Morishita Alone, or with Hellums, Renders the Claimed Invention Obvious

It is further respectfully submitted that the invention as defined in claims 4, 18 and 21 – 24 is not obvious over Morishita alone or in view of Hellums (5,362,988). The invention defined in claim 4 is dependent on that defined in claim 1, the invention of claim 18 and 21 – 24 dependent on claim 16. Neither Morishita alone nor in combination with Hellums discloses the bypass or enable signal responsive to a signal from the host that power up is complete.

Hellums is cited from the proposition that a transistor (28) "... is made of a plurality of transistors for the purpose of increasing the pull up speed." While this may be true in the case of Hellums, as cited above, the size of transistor 1h is disclosed to be limited, and indeed specifically made small for a particular purpose. (See Col 15 line 69 – col.16 line13, quoted above).

Hence, Morishita specifically and explicitly teaches away from any combination of the Hellums transistor with its teachings.

It is there for respectfully submitted that claims 4, 18 and 21 – 24 are not obvious in view of Morishita or Hellums.

Based on the above amendments and these remarks, reconsideration of claims 1-36 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

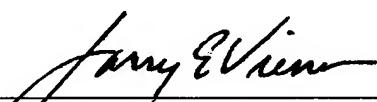
Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including today, March 28, 2005.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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By:


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